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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------------|------------------|
| 10/774,265 | 02/06/2004 | Bernd Laquai | 860-011679-US(PAR)/200211 | 8659 |
| 2512 | 7590 | 06/07/2005 | EXAMINER | |
| PERMAN & GREEN 425 POST ROAD FAIRFIELD, CT 06824 | | | SUAREZ, FELIX E | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2857 | |
| DATE MAILED: 06/07/2005 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|--|--------------------------------------|--------------------------------------|--|
| <p align="center">Office Action Summary</p> | Application No. 10/774,265 | Applicant(s) LAQUAI, BERND | |
| | Examiner Felix E. Suarez | Art Unit 2857 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 9 and 12-15 is/are rejected.
- 7) ☒ Claim(s) 4-8, 10 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>17Feb04; 11Jun2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-3, 9 and 12-15 are rejected under 35 U.S.C. 102(e) as being unpatentable over Choudhary (U.S. Patent No. 6,782,404).

With respect to claims 1 and 15, Choudhary teaches a method (or a program storage medium) for determining the amount of deterministic jitter and random jitter in a digital signal having transitions between logical levels, the method comprising the steps of:

- a) determining a plurality of bit error rate values (see col. 4, lines 5-14 and col. 7 line 64 to col. 8 line 5), each bit error rate value being associated with one of a plurality of successive timing points (see col. 3, lines 37-46),
- b) applying a polynomial fit to said plurality of bit error rate values associated with said timing points for determining a number of polynomial coefficients of said polynomial fit (see col. 5, lines 13-39 and col. 7, line 56 to col. 8 line 5), and
- c) deriving (see col. 5, lines 40-53) the amount each of said deterministic and said random jitter from said polynomial coefficients (see col. 3, lines 21-26 and col. 7, lines 19-28).

With respect to claim 2, Choudhary further teaches that, each bit error rate value is derived from a comparison of a result of a detection of a transition occurring in the digital signal cumulatively prior to its associated timing point with an expected signal (see col. 7 line 64 to col. 8 line 5).

With respect to claim 3, Choudhary further teaches, said polynomial fit is applied to said plurality of bit error rate values with respect to the time coordinate (see col. 3, lines 37-46).

With respect to claim 9, Choudhary further teaches, said polynomial fit to said bit error rate values is performed by means of linear regression (see col. 6, lines 47-63).

With respect to claim 12, Choudhary further teaches, said polynomial fit is of second order (see col. 6, lines 27-39).

With respect to claims 13 and 14, Choudhary teaches, an arrangement for determining the amount of deterministic jitter and random jitter in a digital signal having transitions between logical levels (or a bit error rate tester), comprising:

- a measurement unit for determining a plurality of bit error rate values (see col. 4, lines 5-14 and col. 7 line 64 to col. 8 line 5), each bit error rate value being associated with one of a plurality of successive timing points (see col. 3, lines 37-46),

- a data processing unit capable of applying a polynomial fit to said plurality of bit error rate values associated with said timing points for determining a number of polynomial coefficients of said polynomial fit, and for deriving the amount each of said deterministic and said random jitter from said polynomial coefficients (see col. 5, lines 13-39 and col. 7, line 56 to col. 8 line 5).

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2. Claims 4-8, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Prior Art

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Demir et al. [U.S. Patent No. 6,167,359] describes a phase noise and timing jitter.


Philips et al. [U.S. Patent No. 6,597,727] describes a bit error rate.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felix Suarez, whose telephone number is (571) 272-2223. The examiner can normally be reached on weekdays from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306 for regular communications and for After Final communications.

May 20, 2005

F.S.


HAL NACHTSMAN
PRIMARY EXAMINER
AC 2857